

REMARKS

STATUS AND DATE  
OF ACTION

Claims 1-14 are pending in the application. The Examiner's reconsideration of the objection and rejections in view of the amendments and remarks is respectfully requested.

Applicant appreciates the Examiner's indication that claims 6-14 are allowed and that claim 2 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 1 has been objected to for an informality. Claim 1 has been amended in accordance with the Examiner's suggestion, deleting the word "is" from line 23. Reconsideration of the objection is respectfully requested.

Claim 1 has been rejected under 35 U.S.C. §102(b) as being anticipated by Christiansen, U.S. 5,961,614. The Examiner stated essentially that Huang teaches all the limitations recited in claim 1.

Under 35 U.S.C. 102, a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. The identical invention must be shown in as complete detail as is contained in the claim. See MPEP §2131. It is respectfully submitted that at the very minimum, Christiansen is legally deficient to establish a *prima facie* case of anticipation of claim 1.

Claim 1 recites, *inter alia*, "a central processing unit (CPU) which stores the information on packet data in each of the plurality of buffer descriptors, and allots a flag bit to each buffer descriptor indicating whether a buffer descriptor is being organized, whether an error occurred in packet data received via the plurality of communication channels, or whether the organization of each of the buffer descriptors is completed."

Christiansen teaches that an I/O controller requests the status information contained in the status registers in the Ethernet controller, and that the Ethernet controller sends the status information to the I/O controller which writes the status information on to the end of the received packet (see col. 6, lines 4-16). Christiansen does not teach that a CPU allots a flag bit to each buffer descriptor indicating whether a buffer descriptor is being organized, whether an error occurred in packet data received via the plurality of communication channels, or whether the organization of each of the buffer descriptors is completed, essentially as claimed in claim 1. Christiansen teaches that the status bits can be used for general purpose status and control (see col. 4, lines 9-10). However, Christiansen does not teach that the general purpose status and control includes indicating whether a buffer descriptor is being organized, whether an error occurred in packet data received via the plurality of communication channels, or whether the organization of each of the buffer descriptors is completed. More particularly, Christiansen does not teach that a CPU allots a flag bit to each buffer descriptor indicating whether a buffer descriptor is being organized, essentially as claimed in claim 1. There is no teaching in Christiansen of a status bit for indicating whether a buffer descriptor is being organized. Therefore, Christiansen fails to teach all the limitations of claim 1. The Examiner's reconsideration of the rejection is respectfully requested.

Claims 3-5 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Christiansen in view of admitted prior art. The Examiner stated essentially that the combination of Christiansen and admitted prior art teach or suggest all the limitations of claims 3-5.

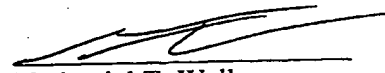
Claims 3-5 depend directly or indirectly from claim 1. The dependent claims are believed to be allowable for at least the reasons given for claim 1. The Examiner's reconsideration of the rejection is respectfully requested.

For the forgoing reasons, the application, including claims 1-14, is believed to be in condition for allowance. Early and favorable reconsideration of the case is respectfully requested.

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Respectfully submitted,

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